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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,209	08/22/2001	Paul Dormitzer	100.232US01	8733

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EXAMINER
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NGUYEN, HAI L

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/935,209

Applicant(s)

DORMITZER ET AL.

Examiner

Hai L. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-10, 12-15, 17-19, 21, 22, 24-27 and 29-32 is/are rejected.
- 7) ☒ Claim(s) 5, 11, 16, 20, 23 and 28 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 04/11/03.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment received on 01/12/04 has been reviewed and considered with the following results:

As to the objections to the specification, Applicant's amendment has overcome the objections, as such; the objections have been withdrawn.

As to the rejections to claim 32, under 35 U.S.C. 112, 1st paragraph, Applicant's amendment has overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to the claims, Applicant's arguments with respect to the prior art rejections have been fully considered but are not deemed to be persuasive. Therefore, the rejections are retained and repeated for the following reasons. In addition, a new action on the merits necessitated by the amendments of claims 30 and 32.

The response to Applicant's arguments is addressed as set forth below.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 7, 12, 17, and 31, remain rejected, as per the previous Office Action, under 35 U.S.C. 102(b) as being anticipated by Nishimura (US 5,990,715; previously cited).

With regard to claim 1, Nishimura discloses in Fig.2 an inherent clock compensation circuit, comprising a clock synchronization circuit coupled to receive an input clock signal (1), wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal logic clock signals (S2, S3); a phase comparator (31) coupled to receive one (S3) of the plurality of internal logic clock signals and a sample clock (S0) from an associated receiver, wherein the phase comparator generates a control signal based on a phase comparison between the sample clock and the one of the plurality of internal logic clock signals; and an inherent down converter channel (32, 33, 34, 41, 51) coupled to receive each of the plurality of internal logic clock signals (S2, S3) and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal.

Claims 7 and 31 are similarly rejected. Note the above discussion with regard to claim 1.

With regard to claim 12, Nishimura discloses in Fig.2 an inherent clock compensation circuit, comprising an input (1) for receiving an input clock signal; a clock synchronization circuit (21, 30) coupled to receive the input clock signal, wherein the clock synchronization circuit generates a master clock signal (S1) and produces a plurality of internal logic clock signals (S2,S3); a tapped delay line (34) coupled to receive a first one (S2) of the plurality of internal logic clock signals and to generate a clock signal with a selected delay as an output clock signal; a phase comparator (31) coupled to receive a second one (S3) of the plurality of internal logic clock signals and a sample clock (S0) from an associated receiver and to generate a control signal based on a phase comparison of the second one of the plurality of internal logic clock signals and the sample clock; and a down converter channel (32, 33, 34, 41, 51) coupled to

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receive the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the second one of the plurality of internal logic clock signals based on the control signal.

Claim 17 is similarly rejected. Note the above discussion with regard to claim 12.

4. Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Burch et al. (US 5,680,422).

With regard to claim 32, Burch et al. discloses in Fig.3 an inherent clock compensation circuit comprising an inherent phase alignment circuit which includes a phase comparator (56) coupled to receive a first clock signal (54) and a sample clock (59) from an associated receiver wherein the phase comparator generates a control signal (60); and a multiplexer to receive first and second data signals (57, 72) and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal (see column 2, lines 21-65).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 21, 24, and 27 remain rejected, as per the previous Office Action, under 35 U.S.C. 103(a) as being unpatentable over Nishimura.

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With regard to claims 21 and 27, the above discussed circuit of Nishimura meets all of the claimed limitations except that Nishimura discloses only one set of circuit instead of a plurality of circuits as called for in claim 21. It would have been obvious to one of ordinary skill in the art to duplicate the clock compensation circuit taught by Nishimura for providing a synchronous system that is required more than one circuit module.

Claim 24 is similar rejected. Note the above discussion with regard to claim 12.

7. Claims 2-4, 6, 8-10, 13-15, 18, 19, 22, 25, 26, and 29, remain rejected, as per the previous Office Action, under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Riordan et al. (US 5,317,601; previously cited).

With regard to claim 2, the above discussed circuit of Nishimura meets all of the claimed limitations except for the limitation that the clock synchronization circuit comprises a phase-locked loop (103 in instant Fig.1) coupled to receive the input clock signal and to generate the master clock signal; and a clock divider (104) coupled to receive the master clock signal and to produce the plurality of internal logic clock signals. Riordan et al. teaches in Fig.2 a circuit having a circuit having a phase-locked loop (40) coupled to receive the input clock signal and to generate the master clock signal; and a clock divider (45) coupled to receive the master clock signal and to produce the plurality of internal logic clock signals as recited in the claim.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize the circuit taught by Riordan et al. with the prior art (Fig.2 of Nishimura) for the advantage of providing a number of precisely synchronized clock signals.

With regard to claim 3, inherently one of plurality of internal logic clock signals is matched in frequency to the sample clock.

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With regard to claim 4, the references meet all of the claimed limitations except for the limitation that the synchronization circuit receives an input clock signal on the order of 100 MHz and produces internal logic clock signals on the order of 20 MHz, 40 MHz, and 100 MHz. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to operate the synchronization circuit with certain frequencies for meeting specific condition which is in each case optimally matched to its application.

Claims 6, 25, and 26 are rejected for similar motivation. Note the above discussion with regard to claims 1 and 4.

Claims 8-10, 13-15, 18, 19, 22, and 29 are similarly rejected. Note the above discussion with regard to claims 2-4.

8. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura in view of Riordan et al.

The above discussed, regard to claim 1, the circuit of Nishimura meets all of the claimed limitations except that the plurality of internal logic clock signals (S2, S3) of Nishimura are not different frequencies. Riordan et al. teaches in Fig.2 a synchronization circuit generates a plurality of internal logic clock signals of different frequencies (PLL1x, 1x, 2x, 4x, Sync4x) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to implement that teaching with the prior art (Fig.2 of Nishimura) to generates a plurality of internal logic clock signals of different frequencies in order to provide a number of precisely synchronized clock signals having different frequencies to meet the demand of many different functional portions of the circuit.

***Response to Arguments***

9. Applicant's argument that the Nishimura reference does not teach "a down converter channel coupled to receive each of the plurality of internal logic clock signals" is not persuasive because Fig.2 of Nishimura clearly shows that the inherent down converter channel (32, 33, 34, 41, 51) receives each of the plurality of internal logic clock signals (S2, S3), which are generated from the input clock signals (1) by the clock synchronization circuit (21,30). Thus it should be understood as the down converter channel coupled to receive each of the plurality of internal logic clock signals as recited in the claims 1, 7, 12, and 17. Therefore, the recited claims are clearly anticipated by the reference.

***Allowable Subject Matter***

10. Claims 5, 11, 16, 20, 23, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest a clock compensation circuit (102 in instant Fig.1), and a method of use thereof, comprising: a clock synchronization circuit (110); a phase comparator (120s); and specifically the limitation directed to a down converter channel coupled to receive each of the plurality of internal logic clock signals and the control signal and to pass data in phase with the sample clock using the one of the plurality of internal logic clock signals based on the control signal, wherein the down converter channel comprises a first flip flop circuit (130) coupled to receive the one of the plurality of internal logic clock signals (105) and to pass a first data signal with a first phase; a second flip flop circuit (132) coupled to receive



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the one of the plurality of internal logic clock signals and to pass a second data signal 180 degrees out of phase with the data signal output by the first flip flop; and a multiplexer (134) coupled to receive the first and second data signals and the control signal, the multiplexer selectively outputting either the first data signal or the second data signal based on the control signal such that the data signal passed by the multiplexer is in phase with the sample clock signal (PHYRET).

### *Conclusion*

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and

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Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN   
March 23, 2004

  
TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800